TDM over IP/Ethernet Implementation in JumboSwitch®

TC COMMUNICATIONS®

White Paper

TDM over IP/Ethernet Introduction

Over the past few years, packet-switched network (PSN) coverage has become ubiquitous, stimulating a desire for the convergence of all communications services over a unified infrastructure. Ethernet/IP is taking the lead in this convergence as the de facto standard and choice by virtually all global markets including telecommunications. This trend has brought into prominence the concept of a pseudo-wire (PW). A pseudo-wire emulates a native service (e.g., ATM, frame-relay, Ethernet or TDM) but utilizes transport PSN.

TDM over IP/Ethernet is a TDM PW technology that makes it possible to provision E1, T1, E3, T3, STS-1 and serial data services across IP, MPLS or layer 2 Ethernet Networks. The services are provided in a manner transparent to all protocols and signaling. TDM over IP/Ethernet enables service providers to migrate to next-generation networks while continuing to provide all their revenue-generating legacy voice and data services, and without fork-lift upgrades of end-user equipment.

TDM over IP/Ethernet also benefits data carriers by enabling them to offer lucrative leased-line and voice services on their packet-switched infrastructures. Furthermore, it enables enterprises to run voice and video over the same IP/Ethernet-based network that is currently used to run only LAN traffic, thereby minimizing network maintenance and operating costs.

Unlike other traffic types that can be carried over pseudo-wires, TDM is a real-time bit stream which causes TDM over IP/Ethernet to have unique characteristics. In addition, conventional TDM networks have numerous special features, particularly those required to carry voice grade telephony channels. These special features imply signaling systems that support a wide range of telephony functions, a rich standardization literature and well developed OAM mechanisms. All of these factors must be taken into account when emulating TDM over PSNs.

One critical issue in implementing TDM pseudo-wires is the clock recovery. In native TDM networks the physical layer carries highly accurate timing information along with the TDM data, but when emulating TDM over PSNs, this synchronization is absent. TDM timing standards can be exacting, and conformance requires innovative mechanisms to adaptively reproduce the TDM timing. These innovative mechanisms are the essence of 3rd generation clock recovery technology. This advanced technology also ensures that recovered clock jitter and wander levels conform to ITU-T G.823/824, even for networks that introduce high packet delay variation and packet loss.

TDM over IP/Ethernet can support all applications that run over E1/T1 circuits. In addition, TDM over IP/Ethernet can provide traditional leased-line services over IP and is transparent to protocols and signaling. Because TDM over IP/Ethernet provides an evolutionary (as opposed to revolutionary) approach, investment protection is maximized.

Implementation of TDM over IP/Ethernet on a Gigabit Multi-Service Access Platform:

The JumboSwitch, an Industrial Grade Gigabit Ethernet platform developed by TC Communications, is currently the only Industrial Switch in the marketplace that provides hot-swappable universal interface card slots for modular interfaces to convert Voice, T1/E1 or Primary ISDN circuits, and serial data, with IP PBX, near Stratum II clock precision and demanding teleprotection speeds.

It consists of a Main card and a Management card as the central control and switching fabrics for the entire unit. This applies to either 4U high or 2U high product versions. Several different interface cards are available for connectivity to TDM-type circuits. For example, the Model TC3845 is designed with TDM over IP/Ethernet technology to interface with T1, E1, T3 or E3 types of TDM circuits. Following are some of the key functionalities implemented on the TC3845 for providing highly accurate T1 / E1 and T3 / E3 services:

Packetization

A high speed hardware engine, SAToP, converts the incoming unframed T1/E1 data flow into IP, MPLS or Ethernet packets and vice versa according to ITU-TY 1413, MEF 8, MFA 8.0.0 and the IETF PWE3 SAToP draft standards.

Latency (Frame Delay):

With various innovative hardware and software designs to handle the jitters and wanders that may result from packet delays and mis-orders, the TC3845 exhibits the best performance for interfacing with T1, E1, T3 or E3 types of TDM circuits. Moreover, one can conclude from extensive testing that the latency is minimal when the subject traffic runs over pure layer 2 Ethernet Switches.

For example, based on both laboratory and actual measurements of 50 JumboSwitches daisy-chained to form a fiber ring, and running at a constant 99% of Gigabit Ethernet traffic, the end-to-end latency measured between two T1 ports is always less than 1 ms without any bit error continuously for 48 hours. (The latency is measured with Anritsu MP1570A SONET/SDH/PDH/ATM Analyzer and verified with JDSU TTC6000A Fire-Berd.)

Frame Delay Variation (FDV):

The TC3845 features several large and configurable jitter buffers which provide sufficient compensation for any packet delay variation that may be introduced by the nature of IP/MPLS/Ethernet networks

Frame Loss and Re-Sequencing:

Because it is important for a TDM over IP/Ethernet or pseudo-wire circuit to handle packets that are out of sequence at receiving ports, the TC3845 performs packet reordering within the range of the jitter buffer. If a packet is lost, packet recovery mechanisms will activate and insert either a pre-determined conditioning value or the last received value. However, this is a rare condition in a well-managed network and the result of such a loss of packets will present itself as a bit error.

Clock Recovery and Synchronization:

Sophisticated TDM clock recovery mechanisms, one for each T1 / E1 interface, is built-in to the TC3845 chip. This allows end-to-end TDM clock synchronization, despite the packet delay variations of the IP/MPLS/Ethernet network.

Clock recovery mechanisms provide both fast frequency acquisition and highly accurate phase tracking. Jitter and wander of the recovered clock are maintained at levels that conform to G.823/G.824 traffic or synchronization interfaces. For TDM clock recovery, the recovered clock performance depends somewhat on the packet network characteristics. The following bullets are the design specifications and verified results on the TC3845 related to Clock Recovery & Synchronization:

1. Short-term frequency accuracy (1 second) on TC3845 is designed to be better than 16 ppb (parts per billion).
2. Capture range is ±90 ppm.
3. Internal synthesizer resolution of 0.5 ppb
4. High resilience to packet loss and mis-ordering, including up to 5% of packet loss/mis-ordering without degradation of clock recovery performance.
5. Robust to sudden significant constant delay changes.
6. Automatic transition to hold-over is performed upon link-break events

In conclusion, the implementation of pseudo-wire on the JumboSwitch platform takes into consideration the latest industrial standards available. Moreover, the JumboSwitch has achieved equal or better performance than pertinent standards as evidenced by rigorous lab testing, both in the laboratory and in actual customer installations.

TC's engineers are completely confident that the 3rd generation clock recovery, meticulously designed circuits and software sub-systems used in the JumboSwitch design, are a perfect fit for modern TDM over IP/Ethernet applications.